ABSTRACT OF THE DISCLOSURE

A semiconductor memory device includes: a memory cell array having a plurality of data select lines disposed in parallel with each other, a plurality of data transfer line disposed in parallel with each other to intersect the data select lines, and electrically rewritable memory cells laid out at cross portions between the data select lines and data transfer lines; a data select line driver for driving the data select lines of the memory cell array; a sense amplifier circuit connected to the data transfer lines of the memory cell array, for performing data read of memory cells selected by one of the data select lines; and a control circuit used for timing control of data read of the memory cell array, for outputting at least two types of timing signals as being different in accordance with a selected data area of the memory cell array.